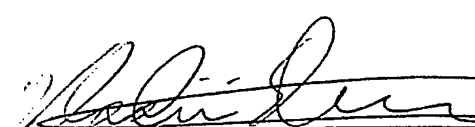




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PTO/SB/33 (07-05)  
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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) P-4007-US	
<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]</p> <p>on _____</p> <p>Signature _____</p> <p>Typed or printed name _____</p>		Application Number 091988, 122	Filed November 19, 2001
		First Named Inventor BLOOM, Ian	
		Art Unit 2812	Examiner BOOTH, Richard A.
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>			
<p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number 43,116</p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34 Registration number if acting under 37 CFR 1.34 _____</p>		<p> Signature Vladimir Sherman Typed or printed name</p> <p>Telephone number Jan 23, 2006 Date</p>	
<p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.</p>			
<p><input type="checkbox"/> *Total of _____ forms are submitted.</p>			

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Attorney Docket No.: P-4007-US

**ARGUMENTS SUBMITTED WITH FORM SB-33**

The Examiner has combined three to four separate and unrelated references in a very crowded field to support his 35 U.S.C. § 103 rejections of the pending claims. In response to Applicant's assertion that there was no motivation to combine the reference and that some of the combinations suggested by the Examiner were improper because they would required an alteration of the inventions taught in the cited reference, the Examiner merely stated that Applicant's arguments were not convincing and that the motivation to combine the reference was clear from his original rejections. Thus, the Examiner has failed to establish a *prima facie* case of obviousness.

More specifically, in the Office Action, the Examiner rejected claims 1,2 and 9 through 15 under 35 U.S.C. § 103(a), as being unpatentable over Eitan et al., U.S Patent 4,758,869, Mitchell et al., U.S Patent 5,120,672, Cheung et al., U.S Patent 6,156,149, Wang., U.S Patent 4,992,391 and Kimura et al., U.S Patent 6,195,196.

Applicants respectfully traverse the rejection of claims 1, 2 and 9 through 15 under the above listed combination of separate and unrelated references on the grounds: (1) that the Examiner hasn't shown any motivation to combine any of the cited references, and (2) even if it were proper to combine the cited references, the combination of the references does not teach or suggest all the claimed limitations of independent claim 1.

As the Examiner should well know, the basic rule of law with regards to obviousness type rejections is that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See also MPEP § 2143 - § 2143.03 for decisions pertinent to each of these criteria.

The Examiner appears to have taken the position that there was some motivation to combine four separate reference relating to four separate areas in the general field of semi-conductors in order to obtain all the limitation of claim 1, which claim recites in part:

“A method of protecting a non-volatile memory device... (1) forming a non-volatile memory device comprising a polycide structure formed over a non-conducting charge trapping layer; and (2) forming a resistive protective layer over at least a portion of said polycide structure, said (3) resistive protective layer adapted to persist on at least a portion of said polycide structure and to absorb electromagnetic wave energy having a wavelength shorter than visible light.”

Contrary to what is claimed, the cited references teach:

1. *Eitan et al.* - **Nonvolatile floating gate transistor**
2. *Mitchell et al.* - **Fabricating a single level merged EEPROM cell having an ONO memory stack substantially spaced from the source region**
3. *Cheung et al.* - **In situ deposition of a dielectric oxide layer and anti-reflective coating**
4. *Wang* - **Process for fabricating a control gate for a floating gate FET**

Although the Eitan reference teaches forming an electromagnetic radiation shielding layer on to a “floating gate” device, both the device structure and the protective material used to protect the structure are substantially different in the Eitan reference than what is claimed. More specifically, Eitan teaches protecting a “floating gate” device using an opaque cover, typically aluminum. Conversely, claim 1 recites the limitations of a “polycide structure formed over a non-conducting charge trapping layer” and a “resistive protective layer adapted to persist on at least a portion of said polycide structure and to absorb electromagnetic wave energy having a wavelength shorter than visible light.” The main distinctions between what is claimed and what is shown in the Eitan reference are:

No.	Eitan Reference	Claim 1
1.	Floating Gate – Conductive Charge	Non – Conducting Charge Trapping Layer

APPLICANT(S): Bloom, Ilan  
SERIAL NO.: 09/988,122  
FILED: November 19<sup>th</sup>, 2001  
Page 3

	Trapping Layer	
2.	Protective Element - opaque cover (typically aluminum)	Protective Element – resistive material
3.	Not Shown	Polycide Structure

The Examiner has asserted that although the above listed elements are absent from the Eitan reference, this defect may be partially cured by combining the Eitan reference with: (1) the Mitchell reference which teaches an Oxide-Nitride-Oxide (ONO) charge trapping layer in memory cell, (2) the Cheung reference which teaches forming a protective layer to absorb light for antireflective purposes, and (3) the Wang reference discloses a non-volatile memory with a polycide structure and an additional layer over the non-volatile memory.

Applicant asserts that the Examiner used impermissible hindsight to reconstruct the Applicant's invention by using the Applicant's structure as a template and selecting elements from the references to fill the gaps (see *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991)). Applicant notes that for the purpose of considering whether a suggested combination may be used to establish implicit teaching, motivation, or suggestion, the references to be combined must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination.

“[T]he test for establishing an implicit teaching, motivation, or suggestion is what the combination of these two statements of Evans would have suggested to those of ordinary skill in the art, the two statements cannot be viewed in the abstract. . . Rather, they must be considered in the context of the teaching of the entire reference.” *In re Kotzab*, 208 F.3d 1352, 54 USPQ2d 1308 (Fed. Cir. 2000)

Applicant respectfully asserts that an adequate consideration of the prior art cited by the Examiner as a whole, could not have been used to establish sufficient implicit teaching, motivation, or suggestion of the present invention.

APPLICANT(S): Bloom, Ilan  
SERIAL NO.: 09/988,122  
FILED: November 19<sup>th</sup>, 2001  
Page 4

More specifically, although the Mitchell reference teaches a non-conducting charge trapping layer (e.g. ONO), there is no suggestion in either Eitan or Mitchell, one of which teaches a "floating gate" device and the other an NROM device, for their teachings to be combined. As is well known in the art, the fabrication and the operation of floating gate and NROM devices are quite different, and transforming one type of device into another is a significant undertaking.

Even if the Examiner had shown sufficient motivation to combine the teachings of Mitchell with those of Eitan, the Examiner admitted that the claimed limitations of a (1) polycide structure and (2) resistive protective layer are absent were still missing. Those limitations the Examiner found in the Wang and Cheung references, respectively. Once again, however, the Examiner failed to explain why one of ordinary skill in the art would combine the teachings of these references with those of Eitan and Mitchell.

Furthermore, the Examiner mistakenly confused the anti-reflective layer of Cheung, which is specifically intended to "reduce inaccuracies caused by the reflection and refraction of incident radiant energy within a photoresist layer used in the patterning of the dielectric layer" with the resistive proactive layer of claim 1 which is explicitly intended to "protect[ing] a non-volatile memory device."

The Examiner also appears to have been mistaken when citing the Cheung reference, which reference teaches the use of polycide for a floating gate device. As mentioned above, floating gate devices have conducting charge trapping layers. Whereas, Claim 1 specifically states the limitation of a "non-conducting charge trapping layer." Given the difference in fabrication technologies used for floating gate and NROM cells, Applicant asserts it would not have been obvious to combine the teaching of Cheung with the other three cited reference in order to obtain all the limitation of claim 1.

In addition, Applicant respectfully asserts that the teachings of the cited references are not sufficient to render the claims *prima facie* obvious, because the proposed modifications that would be necessary in order to construct a device in accordance with the teachings of the primary reference when combined with the teachings of the THREE secondary references, require, *inter alia*, substantial reconstruction and redesign of the elements shown in the

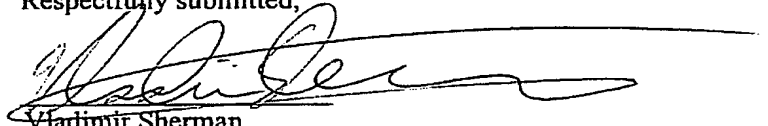
APPLICANT(S): Bloom, Ilan  
SERIAL NO.: 09/988,122  
FILED: November 19<sup>th</sup>, 2001  
Page 5

primary reference (see MPEP 2143.01). In *In re Ratti* the court reversed an obviousness type rejection holding that:

"[the] suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Therefore, Applicant asserts that at least two or more of the four cited references used by the Examiner to support his obviousness rejection may be not be properly combined with the teachings of the others to show all the limitations of claim 1. Even if the combination of all four references was appropriate, the four references combined still fail to teach or suggest all the limitation of claim 1.

Respectfully submitted,



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Dated: January 23, 2006

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